A 2.4-GHz/5-GHz CMOS Low Noise Amplifier with High-Resistivity ELTRAN® SOI-Epi™ Wafers

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Abstract — **The performance of radio frequency integrated circuits (RFICs) in silicon-on-insulator (SOI) technology can be improved by using a high-resistivity SOI substrate. We investigated the correlation between substrate resistivity and the performance of a low noise amplifier (LNA) on ELTRAN SOI-Epi wafers, whose resistivity can be controlled precisely. The use of high-resistivity ELTRAN wafers improves the Q-factor of spiral inductors, and increases the gain and narrows the bandwidth of the LNA.**

I. Introduction

It is widely known that the performance of radio frequency integrated circuits (RFICs) in Si technology can be improved by using high-resistivity Si substrate. Improved RFIC performance in Si bipolar [1], CMOS [2], and silicon-on-insulator (SOI) CMOS [3][4] has been reported. Among the many Si technologies, high-resistivity SOI technology has many advantages, such as full dielectric isolation of devices, low substrate crosstalk, and good low-voltage performance.

The actual substrate resistivity after LSI fabrication processes, however, has not been clarified. It has been reported that substrate resistivity is lowered through SOI wafer fabrication with high-temperature annealing [5]. But, to the authors' knowledge, there has been no report concerning the resistivity after LSI fabrication. Thus, we investigated the correlation between substrate resistivity and the performance of a low noise amplifier (LNA) on SOI wafers with epitaxial layer transfer (ELTRAN) technology, which affords precise control of substrate resistivity [5].

In this paper, we quantitatively report the correlation between substrate resistivity and the performance of an LNA on ELTRAN wafers and show the improvement of LNA performance by using high-resistivity ELTRAN wafers.

II. High-Resistivity ELTRAN Wafers

In the ELTRAN SOI-Epi wafers, an epitaxial layer grown on porous Si is transferred by bonding and etching back porous Si [6]. ELTRAN wafers were fabricated on 200-mm CZ Si wafers with three different resistivities: 0.01-0.02 Ωcm, 10-20 Ωcm, and beyond 1000 Ωcm. The thickness of top Si and buried oxide (BOX) layer were 170 and 500 nm respectively. The substrate resistivity of the three types of ELTRAN was measured by the spread resistance method. Fig. 1 shows the depth profiles of substrate resistivity below the BOX layer before LSI fabrication, and Fig. 2 shows them after the process.

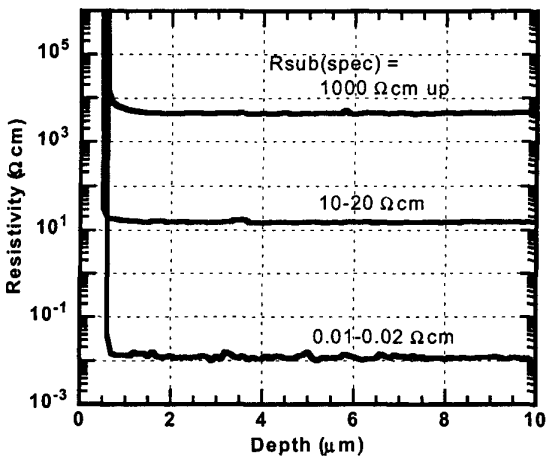

Fig. 1. Depth profiles of the resistivity of ELTRAN wafers before LSI fabrication.

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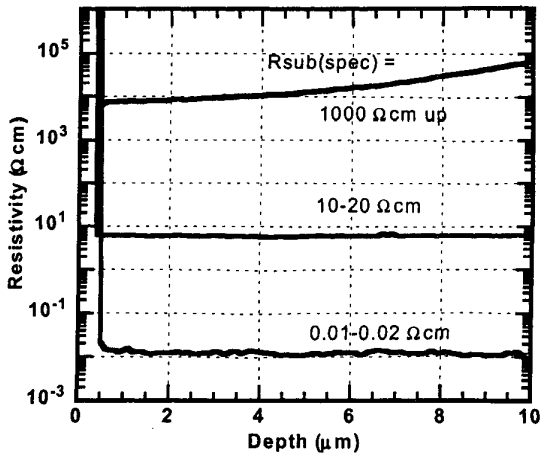

Fig. 2. Depth profiles of the resistivity of ELTRAN wafers after LSI fabrication.

The initial resistivities of the Si wafers were preserved in the ELTRAN wafers before and after the LSI process. Thus, the effects of substrate resistivity on devices and circuits on SOI wafers can be precisely estimated with ELTRAN technology. In the subsequent experiments, we used ELTRAN wafers with resistivity of 10-20 Ωcm (standard ELTRAN) and more than 1000 Ωcm (high-resistivity ELTRAN) because for an RFIC on a low-resistivity substrate the effect of ground plane should also be considered.

III. Spiral Inductors and NMOSFETs in ELTRAN

We fabricated rectangular spiral inductors for RF circuits using a 0.35-μm CMOS process with three-layer AlCu metals. To suppress series resistance, 20-μm-wide ML2-ML3-stacked metal was used for spiral winding, and ML1 was used to access to the internal node of the spiral. The thicknesses of ML1, ML2, and ML3 were 500, 500, and 800 nm, respectively. Fig. 3 shows the inductance L, the series resistance Rs, and the Q-factor of a 3.5-turn spiral inductor fabricated on the standard and high-resistivity ELTRAN wafers. The inductors were made with a 2-port Ground-Signal-Ground configuration for on-wafer S-parameter measurements with a vector network analyzer and air co-planer probes. After de-embedding the influence of open pads from the measured S-parameters, L and Rs were extracted. The Q-factor of the inductor was calculated as

$$Q = \omega L / Rs = - Im(y_{11}) / Re(y_{11}) . \quad (1)$$

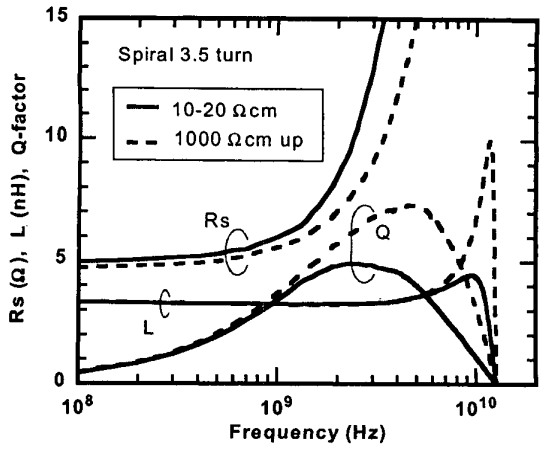

Fig. 3. Characteristics of a 3.5-turn spiral inductor.

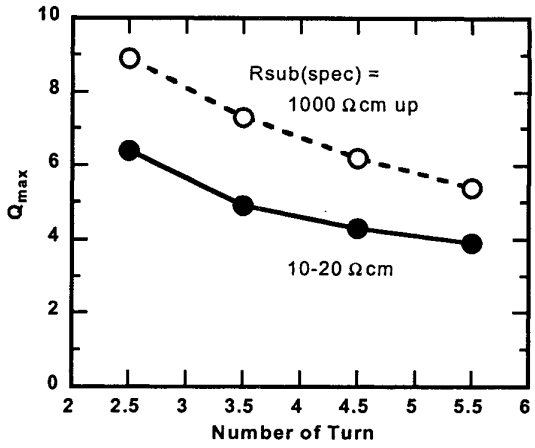

Fig. 4. Maximum Q-factor of the inductors with various turns.

In Fig. 3, The maximum Q-factor of the 3.5-turn inductor on the high-resistivity ELTRAN is higher than that on the standard ELTRAN, because the high-resistivity substrate suppressed the increase of Rs. Fig. 4 shows the Q-factor-improvement for inductors with various turns. The use of the high-resistivity ELTRAN wafer resulted in a 40-% improvement of the Q-factor for all inductors we measured.

We also investigated the characteristics of NMOSFETs fabricated on both types of ELTRAN wafer. There was no difference in the I-V characteristics of the NMOSFETs. Fig. 5 shows the cut-off frequency f_T of NMOSFETs, which have a gate length of 0.35 μm and a total width of 120 μm with a 5-μm-wide multi-finger layout. The NMOSFETs on the high-resistivity ELTRAN have the same f_T as those on the standard ELTRAN. Thus, using

high-resistivity ELTRAN wafers causes no difference in the characteristics of intrinsic NMOSFETs.

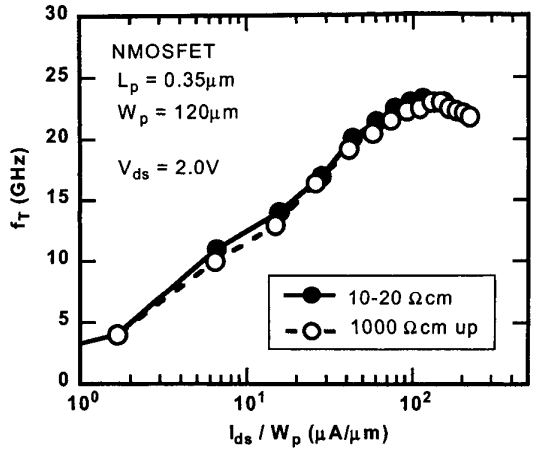

Fig. 5. Cut-off frequency fr of NMOSFETs.

IV. Low Noise Amplifier In ELTRAN

We designed and measured a low noise amplifier (LNA) with the NMOSFETs and spiral inductors described in the previous section. A schematic of the LNA is shown in Fig. 6.

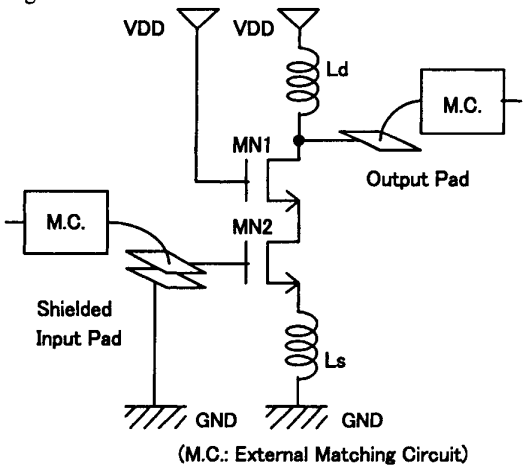

Fig. 6. Schematic of the LNA with external matching circuits.

We adopted a cascoded configuration with two NMOSFETs, MN1 and MN2, for low-power operation. The LNA has a source degenerate inductor, Ls, for adjusting the real part of the input impedance to 50 Ω. An input pad of the LNA has an ML1 shield to suppress the dielectric loss to the Si substrate. A drain choke inductor, Ld, acts as an inductive load to translate modulated source-drain current to output voltage swing. As shown in Fig. 6, input and output impedance were adjusted to 50 Ω, the characteristic impedance of the measurement apparatus, with external matching circuits. The plot of the LNA layout is shown in Fig. 7. The size of the LNA including pads is 0.9 mm x 0.7 mm.

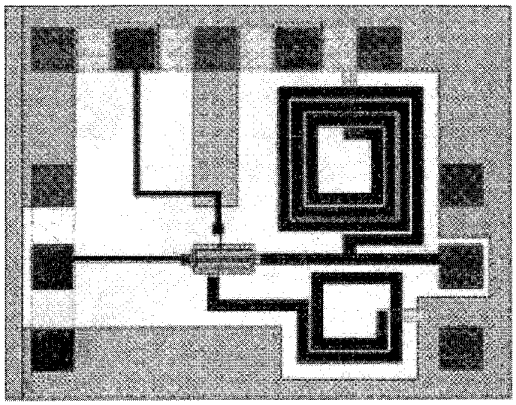

Fig. 7. Plot of the layout image of the LNA.

To evaluate the effect of substrate resistivity on LNA performance, we measured the gain and noise figure (NF) of the LNA with an NF meter and manual tuners. With the tuners, input and output impedance of the LNA were adjusted to 50 Ω at 2.45 or 5.0 GHz. The results are summarized in Table I.

Table I
Summary of LNA performance.

(a) LNA performance tuned on 2.45 GHz

	Vdd (V)	Idd (mA)	Gain (dB)	NF (dB)
standard ELTRAN	2.0	6.1	11.0	2.0
High-Resistivity ELTRAN	2.0	6.2	12.7	1.7

(b) LNA performance tuned on 5.0 GHz

	Vdd (V)	Idd (mA)	Gain (dB)	NF (dB)
standard ELTRAN	2.0	6.1	7.5	2.3
High-Resistivity ELTRAN	2.0	6.2	9.9	2.3

At 2.45 GHz, The gain of the LNA on the high-resistivity ELTRAN is 12.7 dB, which is 1.7 dB higher than that on the standard ELTRAN. The gain increase of the LNA at 5.0 GHz is 2.4 dB, which is clearer than at 2.45 GHz. The reason is that the Q-factor improvement of inductor Ld is

larger at 5.0 GHz than at 2.45 GHz, as shown in Fig. 3. The NFs of the LNA on both ELTRANs are almost same.

To study the substrate effect more quantitatively, we measured the frequency dependence of the LNA gain with a vector network analyzer having a "software fixture" function [7], which converts port impedance by software. With this function, input and output impedance of the LNA can be adjusted to 50 Ω without tuners. Fig. 8 shows output reflection coefficient S_{22} after input and output matching at 2.45 GHz.

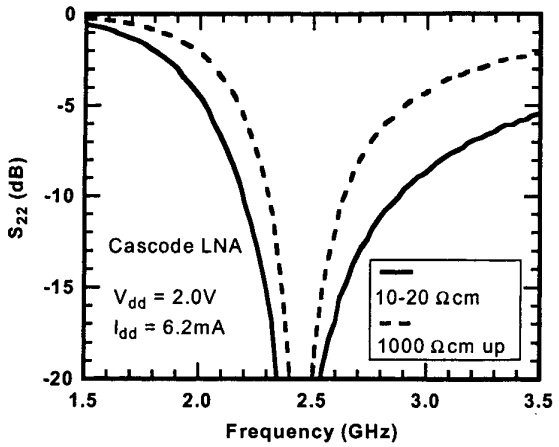

Fig. 8. Output reflection coefficient S_{22} of the LNA.

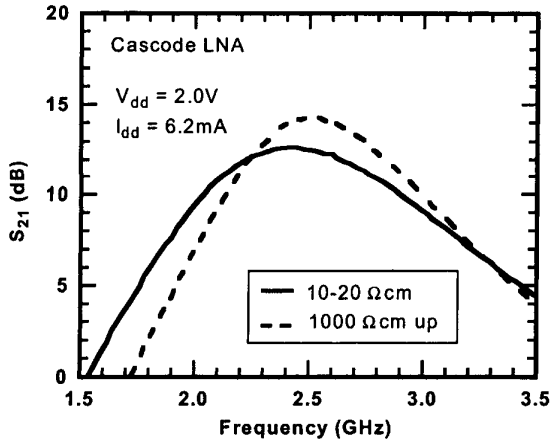

Fig. 9. Forward transmission gain S_{21} of the LNA.

The value of S_{22} at 2.45 GHz is far below –20 dB because the output impedance of the LNA was adjusted to 50 Ω. Note that the bandwidth of the LNA's S_{22} corresponds to the Q-factor of drain inductor Ld. The S_{22} curve of the LNA on the high-resistivity ELTRAN is sharper than that on the standard ELTRAN. Fig. 9 shows the forward transmission gain S_{21} of the LNA on both types of ELTRAN. The LNA on the high-resistivity ELTRAN has 1.5 dB higher gain than that on the standard ELTRAN. This gain increase is almost same as that shown in Table I. Just like in the S_{22} case, the S_{21} curve of the LNA on the high-resistivity ELTRAN has a narrow bandwidth compared with that on the standard ELTRAN. Thus, we conclude that the gain increase and the bandwidth narrowing of the LNA are caused by the Q-factor improvement of the inductor with high-resistivity ELTRAN wafers.

V. Conclusion

We investigated the correlation between substrate resistivity and the performance of an LNA on ELTRAN wafers, which afford precise resistivity control. The use of high-resistivity ELTRAN wafers improved the Q-factor of spiral inductors. The Q-factor improvement of the inductor resulted in a gain increase and bandwidth narrowing of the LNA on a high-resistivity ELTRAN wafer.

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